# CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

**Department of Electrical and Computer Engineering**

# ECE 526L

# 

# LAB – 4: Model of an edge triggered flip/flop using a hierarchal modelling.

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**INTRODUCTION**:

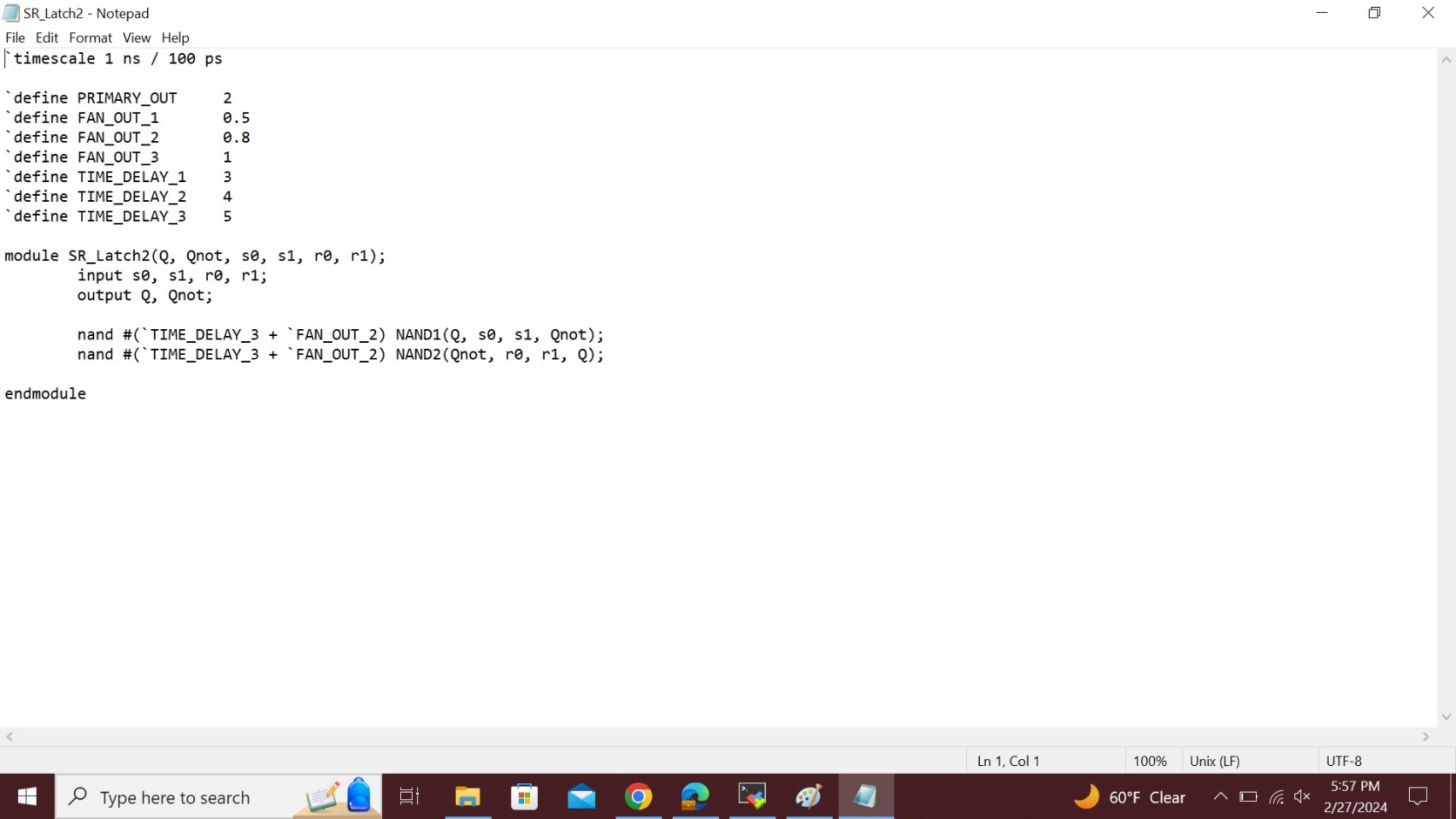
In this lab, we modelled an edge triggered flip-flop using a hierarchal modelling approach using **Synopsys VCS** in **Linux OS** environment and different terminal commands.

**METHODOLOGY**:

The first thing is being familiar with the Linux and Synopsys VCS, that will navigate your system using terminal. Now to write a Verilog code for the module using a text editor, always use Linux based text editors and the file should have **“.v”** extension.

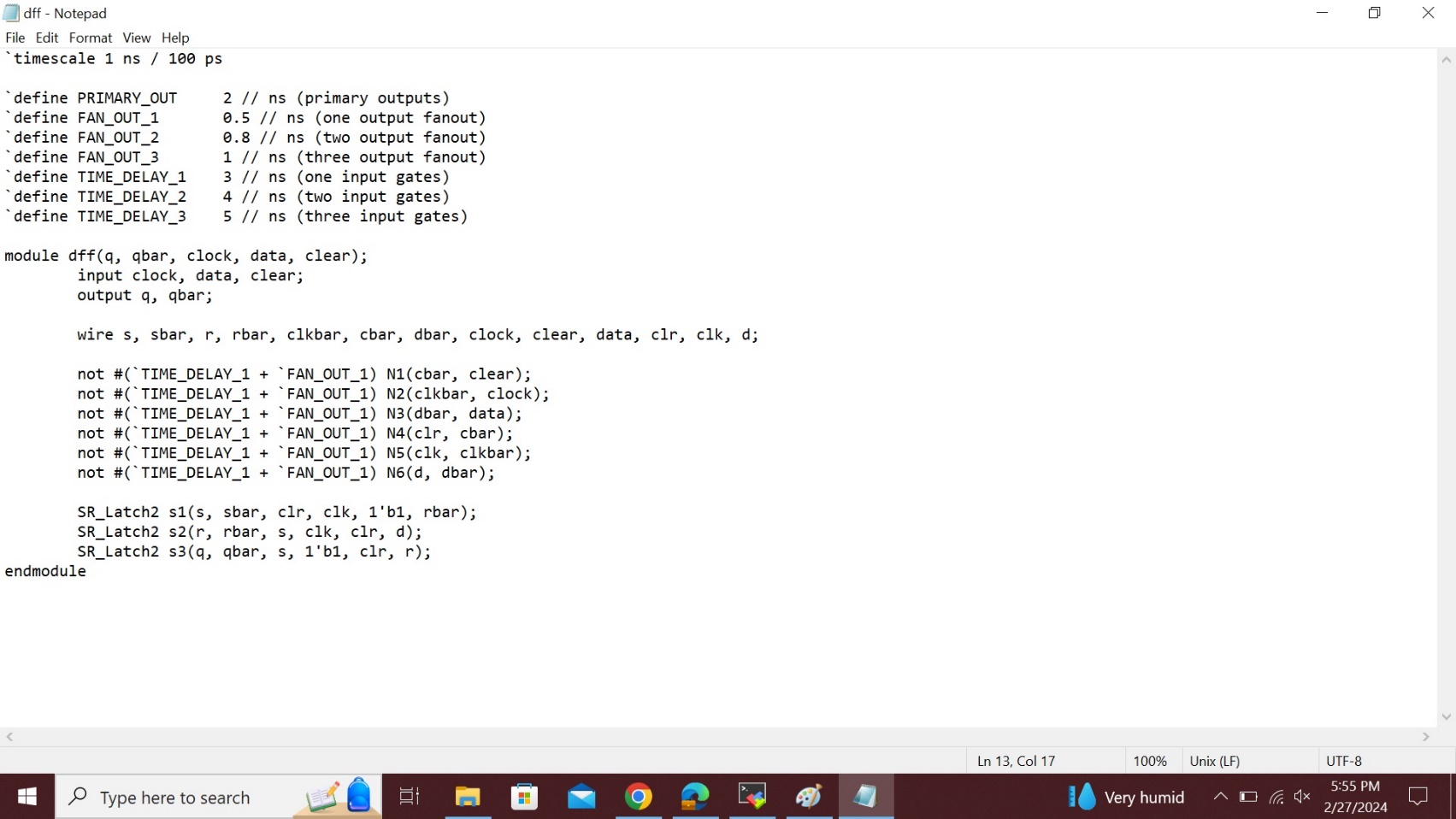
In this lab, we will model an edge triggered flip-flop using a hierarchical modelling approach by using primitive gates in this question and we will write a code for **SR\_latch**. And now save as **“SR\_Latch2”**.

The module name and file name should be consistent,



This is the fig of **“SR\_Latch2”**, store it in new file, also in folder **“Lab4”**.

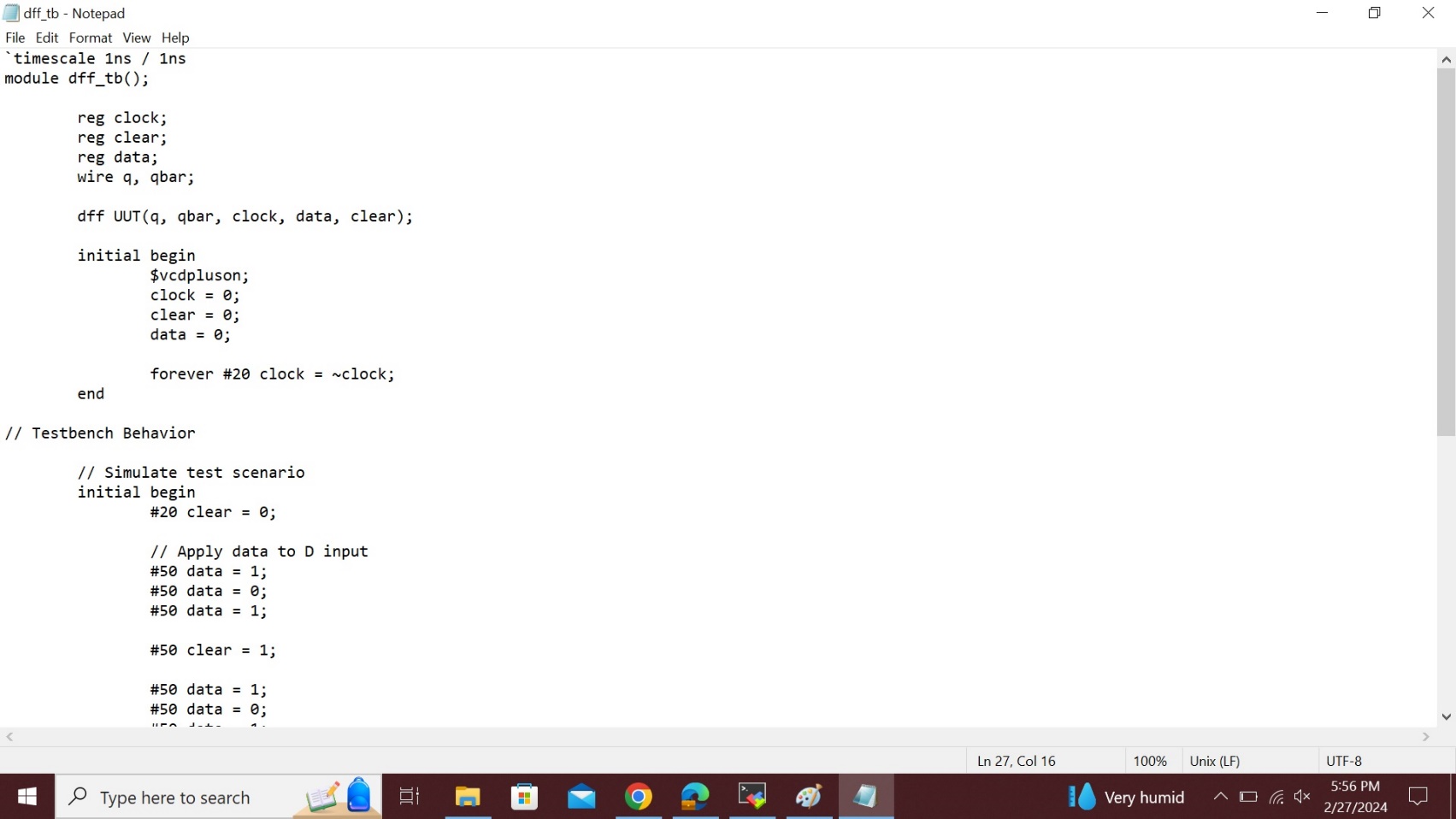
Now for D-flip flop circuit,write the code using above module SR Latch for design of D- flip flop and save it as “dff.v”

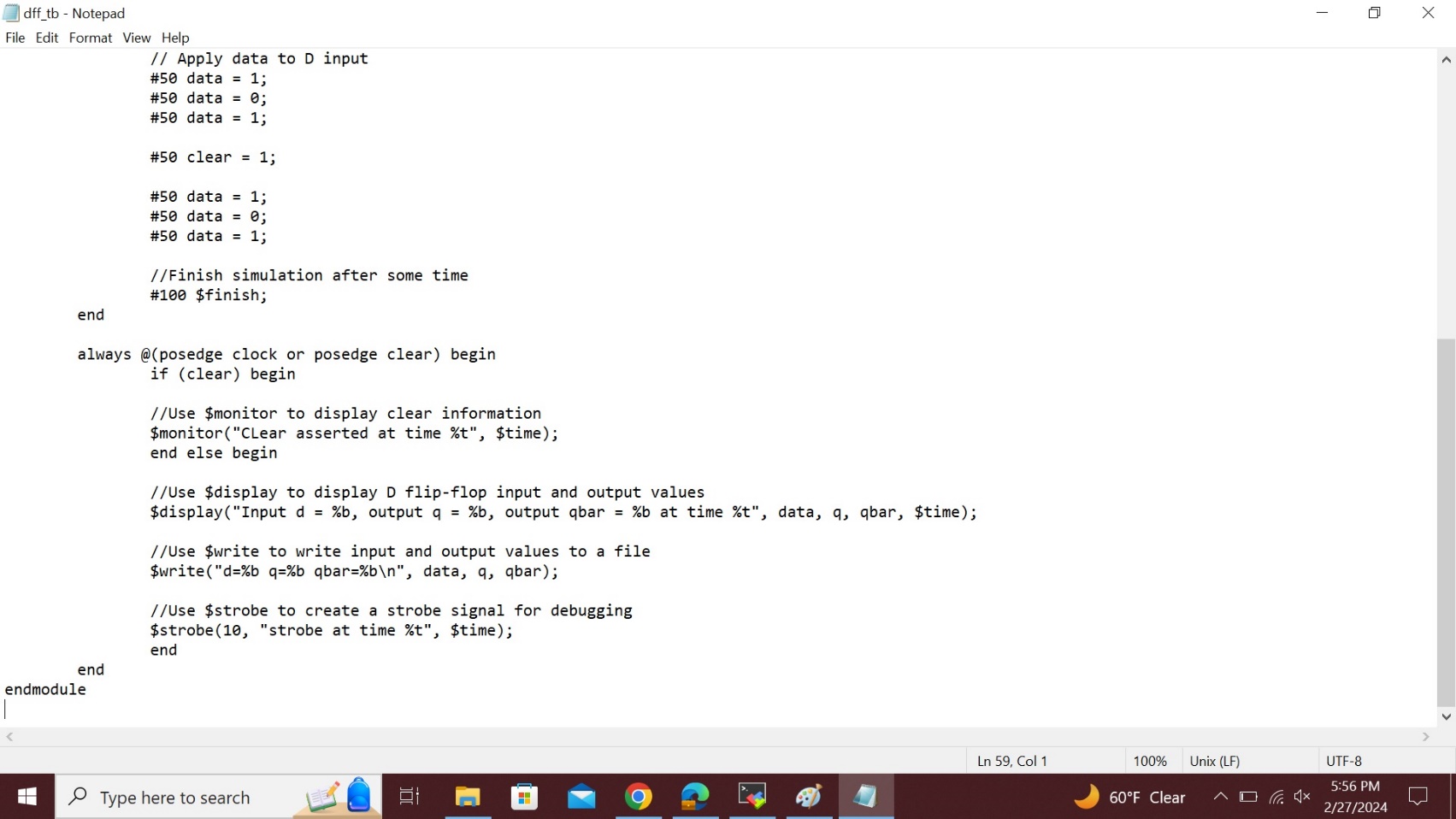


The above figure is the **“dff.v”** deisgn code.

Then we should write a test bench module to verify the functionality of your flip-flop, in this module we use each of the output system tasks, **$monitor, $display**, **$write** and **$strobe** and name it as **“dff\_tb.v”**.

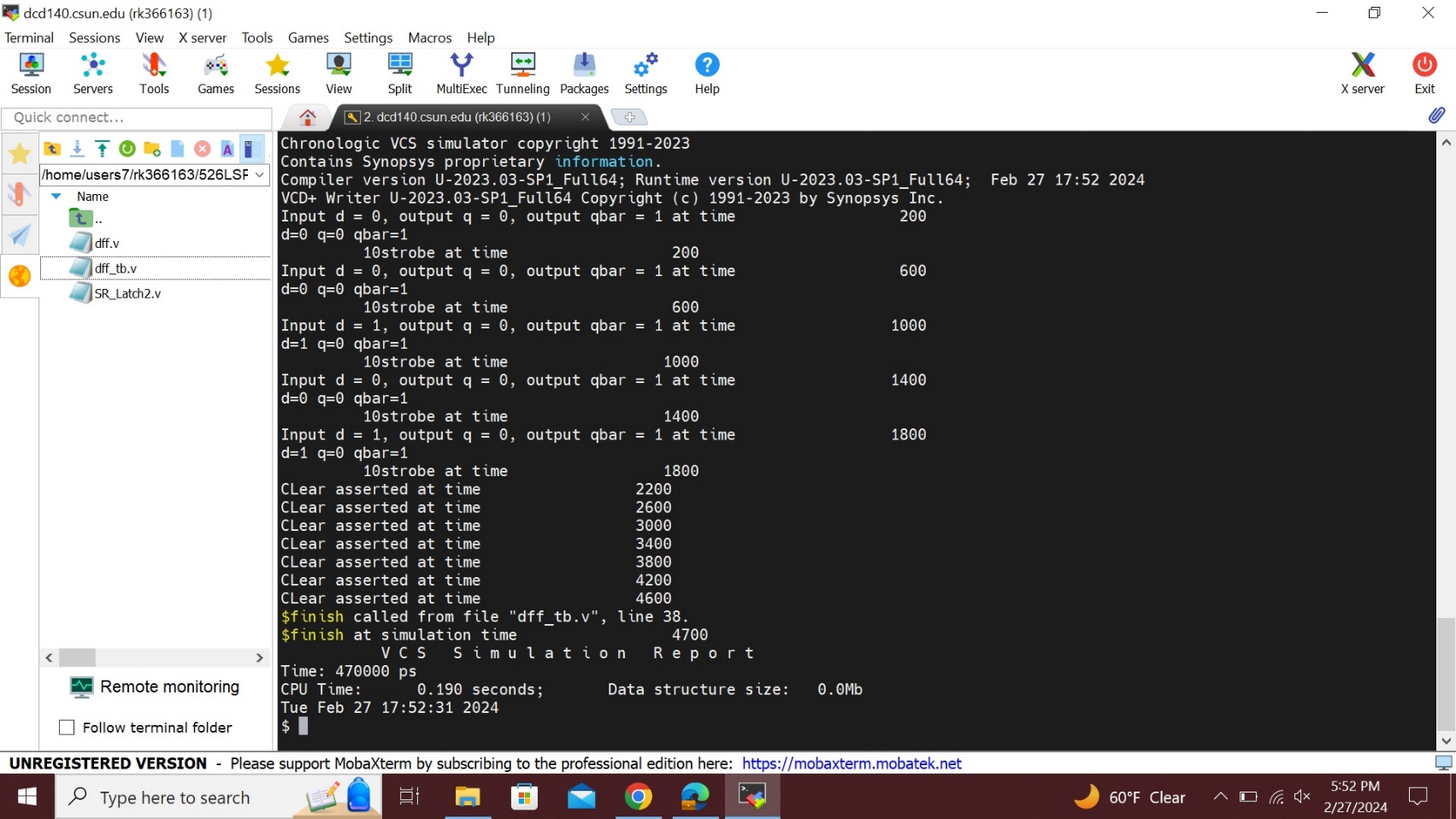
This below is **“dff\_tb.v”** test bench code.



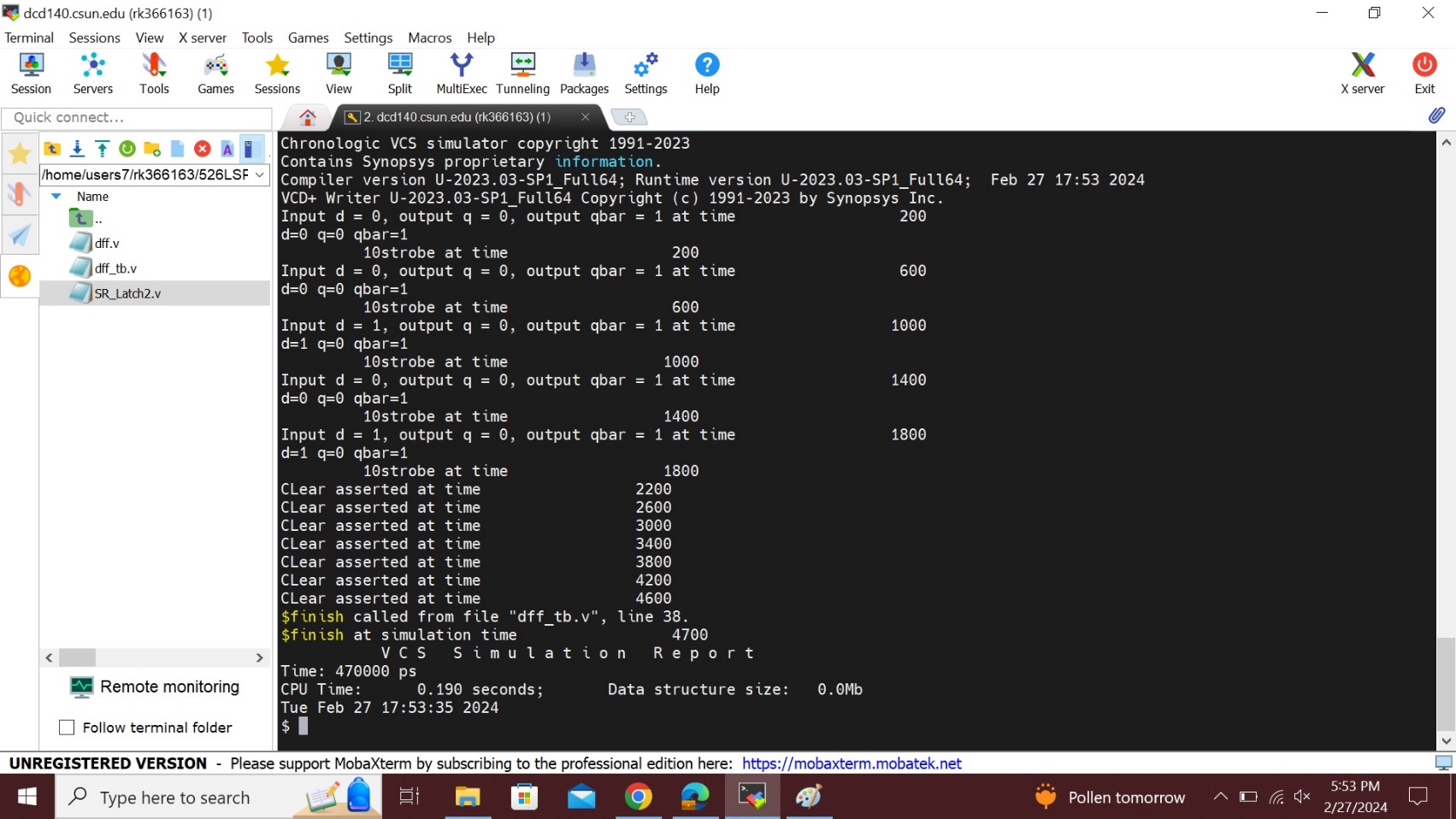


Now, after saving the SR Latch and D-flip/flop. Then, use the command as follows, **“vcs -debug\_access+all SRLatch.v dff.v dff\_tb.v”** If we don’t see any error messages if everything is typed correctly then output should look like below figure;

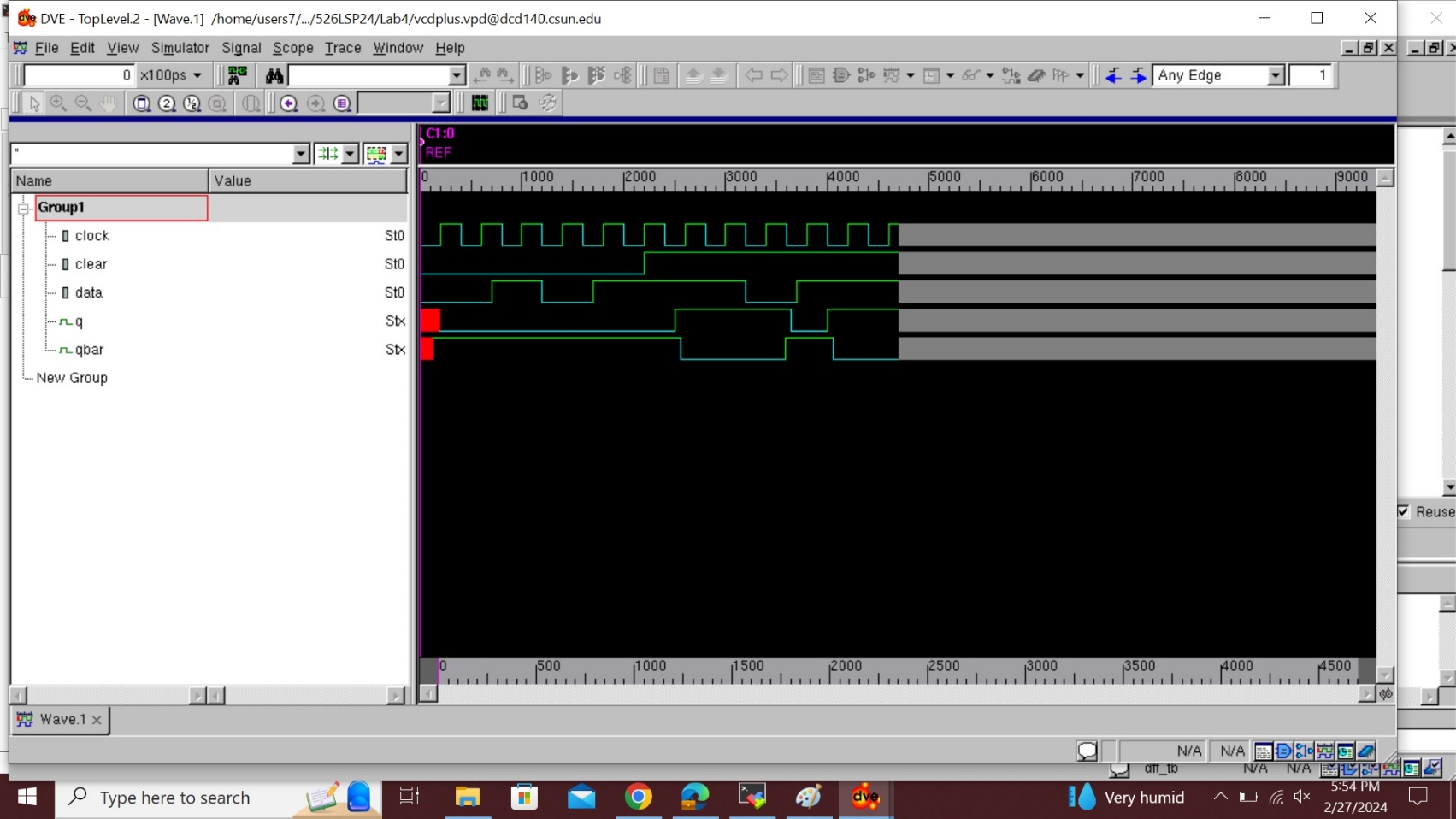
**Simv:**



**Log File Lab4:** Command: **“simv -l Lab4.log”** .



To see the wave form first type **“dve-full64”** in command line, then we will get the blank simulation window, then go to the file and open database then choose **vcdplus.vpd** and open the file. Then finally select all the signals with the mouse, then right click and select to **“add to wave ->new wave view”**.



## Analysis of result:

## The D-Flip/Flop's inputs and outputs are identical, that means the result will be 0 if the input is 0 => 0. Additionally, if the input is 1 => 1, then the output will also be 1. Here, "d" stands for the data input provided by the table mentioned earlier details the D - input as 0, 0, 1, 1 and the 'qbar' output as being identical to the data supplied as 0, 0, 1, 1.

## Furthermore, the data clock will alternate with the letter "q", which will be 0, 1, 0, 1. The D-Flip/Flop completely express what is said in the above waveform, to provide alternative values for the clock, clear, and data, we also use a "NOT" gate here as inverter, which are substitute values for them. Here, the “q” and “qbar” outputs are obtained using the three SR-latches, simply adding the values specified in the code given by the values from the provided circuit. Finally, positive edge triggered d flip/flop becomes active when its clock signal goes from low to high and ignores the high-low transition.

## Conclusion:

## In this lab we done model of an edge triggered flip/flop using a hierarchal modelling approach using Synopsys VCS in Linux OS environment and different terminal commands

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, neither have I allowed nor I will let anyone to copy my work.

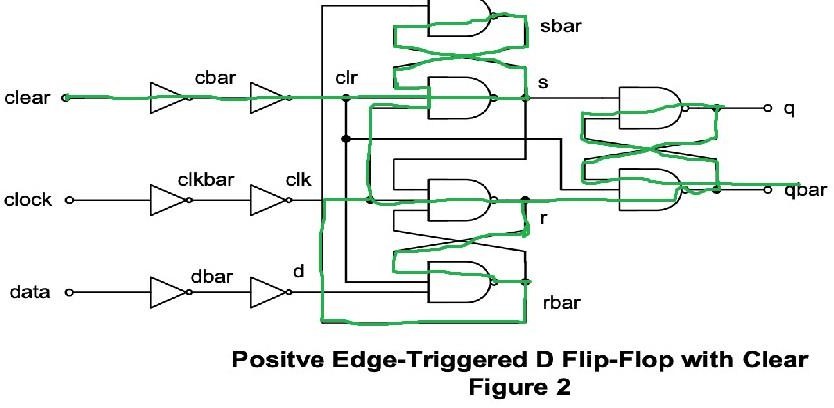
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Name(signed) Raj Kumar

Date 03/01/2024

## Lab Report Solutions:

1. Calculate the longest path delay, show how you calculated it (which gates and what delays) and show the value?

Solution:

The longest path is calculated as

=> NOT + NOT + NAND + NAND + NAND + NAND + NAND + NAND

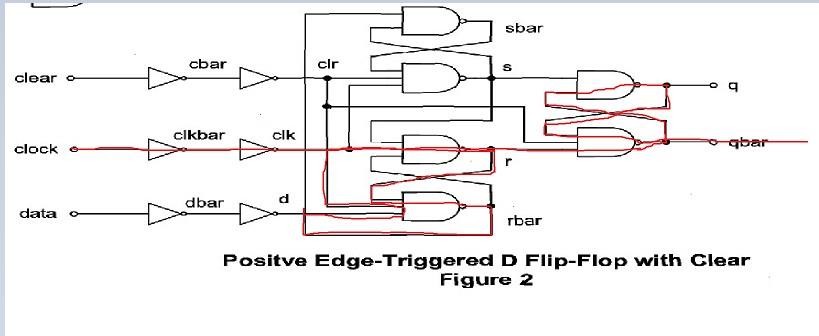
=> (3+0.5) + (3+0.5) + (5+0.8) + (5+0.8) + (5+0.8) + (5+0.8) + (5+1.0) + (5+2.0)

=> 43.2 ns

1. What is the maximum operating frequency for your circuit?

Solution:

It is calculated by 1/ shortest delay  
Clock to qbar :   
=> NOT + NOT + NAND + NAND + NAND + NAND  
=> (3+0.5) + (3+0.5) + (5+0.8) + (5+0.8) + (5+1.0) + (5+2.0) = 31.6ns  
=>1/31.6 = 3.174603175\*10^7



* **Therefore, the above picture is the shortest delay path.**